IN THE CLAIMS

The listing of claims replaces all prior versions, and listings, of claims in the application.

1. (Currently amended) A method comprising:

receiving data on a plurality of data links, the data on at least two respective links being transmitted with a differential transmission delay, such that the plurality of data links includes a slow link having a first transmission delay and at least one other link having a second transmission delay, the first transmission delay longer than the second transmission delay;

~~writing the data in a delay compensation buffer for each data link, the delay compensation buffer having an associated delay corresponding to the first transmission delay~~ writing the data from the slow link to a first delay compensation buffer and the data from the at least one other link to a second delay compensation buffer, wherein a first write pointer for the first delay compensation buffer points to a different location relative to a second write pointer for the second delay compensation buffer; and

reading the data from the delay compensation buffer for each data link faster than the data is written into the buffer.

2. (Original) The method of claim 1, wherein the receiving the data includes receiving an asynchronous transfer mode (ATM) data cell.

3. (Original) The method of claim 1, wherein the receiving data includes receiving the data on one or more T1/E1 data links.

4. (Previously Presented) The method of claim 1, further comprising:

deleting the slow link such that the delay caused by the slow link is reduced.

5. (Previously Presented) The method of claim 4, further comprising:

adding a fast link, having a transmission delay less than the second transmission delay, after the slow link is deleted and the transmission delay resulting from the slow link is reduced.

6. – 10. (Canceled)

11. (Currently amended) A machine-readable medium that provides instructions, which if executed by a processor, cause the processor to perform an operation comprising:

receiving data on a plurality of data links, the data on at least two respective links being transmitted with a differential transmission delay, such that the plurality of data links includes a slow link having a first transmission delay and at least one other link having a second transmission delay, the first transmission delay longer than the second transmission delay;

~~writing the data in a delay compensation buffer for each data link, the delay compensation buffer having an associated delay corresponding to the first transmission delay~~ writing the data from the slow link to a first delay compensation buffer and the data from the at least one other link to a second delay compensation buffer, wherein a first write pointer for the first delay compensation buffer points to a different location relative to a second write pointer for the second delay compensation buffer; and

reading the data from the delay compensation buffer for each data link faster than the data is written into the buffer.

12. (Original) The machine-readable medium of claim 11, further providing instructions, which if executed by the processor, cause the processor to perform an operation comprising:

receiving an asynchronous transfer mode (ATM) data cell.

13. (Original) The machine-readable medium of claim 11, further providing instructions, which if executed by the processor, cause the processor to perform an operation comprising:

receiving the data on one or more T1/E1 data links.

14. (Previously Presented) The machine-readable medium of claim 11, further providing instructions, which if executed by the processor, cause the processor to perform an operation comprising:

deleting the slow link such that the delay caused by the slow link is reduced.

15. (Previously Presented) The machine-readable medium of claim 11, further providing instructions, which if executed by the processor, cause the processor to perform an operation comprising:

adding a fast link, having a transmission delay less than the second transmission delay, after the slow link is deleted and the transmission delay resulting from the slow link is reduced.

16. (Currently amended) A system for inverse multiplexing over an asynchronous transfer mode (ATM) network comprising:

means for receiving data on a plurality of data links, the data on at least two respective links being transmitted with a differential transmission delay, such that the plurality of data links includes a slow link having a first transmission delay and at least one other link having a second transmission delay, the first transmission delay longer than the second transmission delay;

means for ~~writing the data in a delay compensation buffer for each data link, the delay compensation buffer having an associated delay corresponding to the first transmission delay~~ writing the data from the slow link to a first delay compensation buffer and the data from the at least one other link to a second delay compensation buffer, wherein a first write pointer for the first delay compensation buffer points to a different location relative to a second write pointer for the second delay compensation buffer; and

means for reading the data from the delay compensation buffer for each data link faster than the data is written into the buffer.

17. (Original) The system of claim 16, wherein the means for receiving the data includes means for receiving an asynchronous transfer mode (ATM) data cell.

18. (Original) The system of claim 16, wherein the means for receiving data includes means for receiving the data on one or more T1/E1 data links.

19. (Previously Presented) The system of claim 16, further comprising:

means for deleting the slow link such that the delay caused by the slow link is reduced.

20. (Previously Presented) The system of claim 18, further comprising:

means for adding a fast link, having a transmission delay less than the second transmission delay, after the slow link is deleted and the transmission delay resulting from the slow link is reduced.